APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: APPARATUS AND METHOD OF PREVENTING CONGESTION IN MESSAGE TRANSMISSION SYSTEM

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APPARATUS AND METHOD OF PREVENTING CONGESTION IN MESSAGE TRANSMISSION SYSTEM

BACKGROUND OF THE INVENTION

[1] This application claims the benefit of Korean Application No. P2000-86398, filed on December 29, 2000, which is hereby incorporated by reference.

1. Field of the Invention

[2] The present invention relates to a message transmission system and, more particularly, to an apparatus and method of preventing data traffic congestion in a message transmission system.

2. Background of the Related Art

[3] In general, a bus access arbiter, of a a master module, arbitrates bus access for transmitting a message from one functional module to another module, in a message transmission system of a private branch exchange system. Additionally, the message is transmitted through a Frame Synchronous (FS) signal, which is generated by a master bus controller. The system is able to provide both a serial and a parallel message transmission method.

[4] FIG. 1 illustrates a message transmission system of a background art, private branch exchange system. The system includes a master module 20 and N slave modules 30_1,

30_2, ... , 30_N. The master module 20 and all of the slave modules are connected to the common bus (CB) 5 and the control line (CL) 10.

[5] There are two ways for the module to connect to the CB 5, a serial line (SL) connection and a parallel line (PL) connection. The SL connection uses only one of the CB lines, and the PL connection uses all of the CB lines. The master module 20 is connected to all of the CB lines. Each of the N slave modules can be connected to the CB 5 using the SL or PL connection. The CL 10 includes a clock signal, a parity error signal, a busy signal, a frame synchronization signal, and many other signals.

[6] Similar to the slave modules 30_1 - 30_N, the master module 20 can make a request for message transmission and is included in a node to communicate a message. Additionally, the master module 20 arbitrates access to the CB 5. The master module 20 shown in FIG. 1 includes a master bus controller 21, a CPU 22, and a shared memory 23, as shown in FIG. 2.

[7] The master bus controller 21 includes a serial/parallel controller 21_1, a message transmitting/receiving controller 21_2, a memory arbiter 21_3, and a bus request arbiter 21_4. In addition, the bus request arbiter 21_4 includes an access authorizing block 21_4a and a request storage 21_4b, as shown in FIG. 3.

[8] Reference will now be made in detail to the method of operating the message transmission system of the background art, private branch exchange system. We know that only one node may use the CB 5 for a given period of time. Therefore, a node must initially obtain a right to access the CB 5, to send a message to another node through the CB 5.

[9] The bus request arbiter 21_4, of the master bus controller 21 shown in FIG. 2, receives an access-requesting signal from each module shown in FIG. 1. Based on this signal, the bus request arbiter 21_4 provides a selected module access to the CB 5.

[10] The request storage 21_4b, of the bus request arbiter 21_4 shown in FIG. 3, stores the access requesting signals, sent by the access requesting modules, in the order that they are received in a given period of time. After all the requesting signals are stored in the request storage 21_4b, the access authorizing block 21_4a gives a bus access approval to a node, which is selected using a given selecting rule.

[11] In addition, the master bus controller 21 provides frame synchronization and clock signals to the slave modules, which they use to send or receive information. Therefore, the slave modules are able to receive the data provided through the CB 5 and determine whether their access request is approved.

[12] When the master bus controller 21 approves the access request of a node, the transmitting node transmits a node number of the receiving node. Thereafter, the receiving node sends information regarding its preferred receiving method to the master module 20, through the CB 5. Then, master module 20 informs the transmitting module of the preferred method. Finally, the transmitting module transmits the message to the receiving module, using the preferred message transfer method (i.e., a serial or parallel transfer method).

[13] However, this method of transmitting a message in a message transmission system of the background art, private branch exchange has several disadvantages. If there is only one node sending an access-requesting signal, the master bus controller 21 gives an access right

immediately after it receives the requesting signal. Then, the node may use all of the bandwidth of the bus. In this case, data traffic congestion may occur in the node. Even a single slave node, having such congestion, may cause the whole system to be unstable.

[14] The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

SUMMARY OF THE INVENTION

[15] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[16] Another object of the present invention is to provide an apparatus and a method of preventing data traffic congestion in a message transmission system.

[17] A further object of the present invention is to prevent traffic congestion by arbitrating access to a common bus so that each module is able to send an access requesting signal only after its previously set standby period has expired.

[18] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of arbitrating access to a common bus for a first set of modules included in a message transmission system includes (a) setting a standby period of each of the first set of modules, (b) identifying a second set of modules whose standby periods are determined to be expired, and (c) allowing each of the second set of modules to send an access-requesting signal.

[19] The method further includes (d) selecting a final module among the second set of modules, using a given selecting rule and (e) sending an acknowledgment signal to the selected final module.

[20] In another aspect of the present invention, a method of arbitrating access to a common bus, for a first set of N modules included in a message transmission system, includes (a) setting P_n to an initial prescaler value and setting I_n to an initial interval value of an nth module, where $n = 1, 2, 3, \ldots N$, and P_n and I_n represent a standby period for the nth module; (b) identifying a second set of modules whose standby periods are determined to be expired using P_n and I_n; and (c) allowing each of the second set of modules to send an access-requesting signal.

[21] In addition, the method further includes (d) selecting a final module, among the second set of modules using a given selecting rule, and (e) sending an acknowledgment signal to the selected final module.

[22] Step (b) may include (b1) down-counting P_1 of a first module, for every first period, and determining whether P_1 is equal to a first predetermined value; (b2) down-counting I_1 of the first module, for every second period, and determining whether I_1 is equal to a second predetermined value, if it is determined in step (b1) that P_1 is equal to the first predetermined value.

[23] Step (b) may further include (b3) treating the first module as one of the second set of modules, if it is determined in the step (b2) that I_1 is equal to the second predetermined value, and (b4) performing steps (b1) to (b3) for the 2nd, 3rd, 4th, ... , Nth modules.

[24] In another aspect of the present invention, an apparatus for arbitrating access to a common bus, for a first set of modules included in a message transmission system, includes a standby period storage storing a standby period of each of the first set of modules; an access authorizing block identifying a second set of modules whose standby periods are determined to be expired and allowing each of the second set of modules to send an access-requesting signal; and a request storage storing an access request made by each of the second set of modules.

[25] The objects of the invention may be further achieved in whole or in part by a method of arbitrating access to a common bus shared by a plurality of modules, including assigning a first value and a second value to each of the plurality of modules; repeatedly decreasing the first value until the first value meets a first condition, for each of the plurality of modules; decreasing the second value and determining whether the second value meets a second condition, for each of the plurality of modules having a corresponding first value that meets the first condition; and transmitting an access request to a bus arbiter, requesting access to the common bus, from each of the plurality of modules having a corresponding second value that meets the second condition.

[26] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[27] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[28] FIG. 1 illustrates a message transmission system of a background art, private branch system;

[29] FIG. 2 illustrates the master module, shown in FIG. 1, in greater detail;

[30] FIG. 3 illustrates the bus request arbiter, shown in FIG. 2, in greater detail;

[31] FIG. 4 illustrates a bus request arbiter included in a master bus controller of the present invention;

[32] FIG. 5 illustrates an interval value table included in the interval value storage, shown in FIG.4; and

[33] FIG. 6 illustrates a method of arbitrating access to a common bus, for a set of modules included in a message transmission system, according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[34] FIG. 4 illustrates a bus request arbiter 400, included in a master bus controller of the present invention. The bus request arbiter 400 includes an access-authorizing block 42, a request storage 44, and an interval value storage 46.

[35] The interval value storage 46 stores a prescaler value P_n and an interval value I_n of an n^{th} slave module. Both values, which are initially set by a user for each slave module, are used to stop the respective slave module from re-accessing the common bus before its given

standby period has expired. The interval value storage 46 contains an interval value table that stores an address of the n^{th} slave module, P_n, I_n, a P-counter, and an I-counter, for each slave module. The table is shown in FIG. 5.

[36] The access-authorizing block 42 reads P_n and I_n of each slave module, stored in the interval value storage 46, and determines whether a given standby period has expired for the respective slave module, by down-counting the stored values of P_n and I_n.

[37] The request storage 44 stores the access requesting signals, which are sent by each access requesting module, in the order that they are received, for a given period of time.

[38] FIG. 6 illustrates a method of arbitrating access to a common bus (CB), for slave modules included in a message transmission system of the present invention. The access-authorizing block 42 identifies a set of slave nodes, whose predetermined standby periods are expired, among the original set of slave nodes that may access the CB. The access authorizing block 42 accomplishes this by performing steps S61 to S65, as described below, for each of the originally identified set of slave nodes.

[39] A system user initially sets P_n and I_n for a slave module (S61). If the interval value I_n of a slave module is set to zero, the access-authorizing block 42 will not give an access right to the slave module.

[40] Next, the access authorizing block 42 reads the prescaler and interval values of the slave module and stores the values in its built-in memory. Then, the access authorizing block 42 down-counts the stored prescaler value for every given period (S62). Thereafter, the access authorizing block 42 checks whether the down-counted prescaler value is zero (S63), and

it repeats step S62 until the down-counted prescaler value becomes zero. When it is finally determined, in step S63, that the prescaler value is zero, the access authorizing block 42 down-counts the interval value stored in the built-memory (S64).

[41] Next, the access authorizing block 42 checks whether the down-counted interval value is zero (65). If it is not, access authorizing block 42 re-accesses the interval value storage 46 and resets its current prescaler value, stored in the built-in memory of the access authorizing block 42, to the original prescaler value stored in the interval value storage 46. Then, the access authorizing block 42 repeats steps S62 to S65 until the interval value becomes zero.

[42] When it is finally determined, in step S65, that the interval value is zero, the access-authorizing block 42 allows the slave module to send an access requesting signal.

[43] After the access-authorizing block 42 performs steps S61 to S65, for each of the slave nodes that may access the CB, it receives the access-requesting signals from those slave modules whose predetermined standby periods are expired. Then, the access authorizing block 42 performs an arbitration process, based on a given arbitrating rule (e.g., a round robin method) (S66). The access authorizing block 42 selects a slave module using the arbitration rule (S67), and the selected slave module sends a message through the CB (S68).

[44] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses

are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.